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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Samson Huang	Group Art Unit:	2675
Serial No.:	09/493,319	Examiner:	Leland R. Jorgensen
Filed:	January 28, 2000		
For:	OPTICAL DISPLAY DEVICE HAVING A MEMORY TO ENHANCE REFRESH OPERATIONS	Atty. Dkt. No.:	ITL.0312US (P7995)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated December 10, 2003, finally rejecting claims 45-54.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 010554/0968.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit: April 30, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.
Janice Munoz
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III. STATUS OF THE CLAIMS

Claims 45-54 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

An Amendment (copy enclosed) is being filed concurrently herewith to correct a typographical error in claim 45. It is assumed for purposes of this appeal that the Amendment will be entered.

V. SUMMARY OF THE INVENTION

Referring to Fig. 2, an embodiment 50 of an SLM cell in accordance with the invention includes a memory 66 (part of a larger static random access memory (SRAM), for example) that stores a digital indication of a pixel intensity for a pixel cell 54 (of the SLM cell 50). The SLM cell 50 may use a digital-to-analog converter (DAC) 62 to, during a refresh operation, convert the digital indication into an analog voltage to refresh the charge on a capacitor 52 (of the SLM cell 50) that furnishes the terminal voltage to a pixel cell 54 of the SLM cell 50. As an example, in some embodiments, the memory 66 may store eight bits that may indicate up to 256 different pixel intensity levels for the pixel cell 54. Specification, p. 4.

The SLM cell 50 may be one of several SLM cells 50 of a row of an SLM. Due to the above described arrangement, all of the capacitors 52 in the SLM cells 50 of the row may be updated at the same time without coupling any of the capacitors 52 to a tri-

stated bit, or column, line. Therefore, charge sharing between the capacitors 52 and the bit lines of the SLM does not occur, and thus, each capacitor 52 may be smaller than the traditional capacitor of the SLM cell. Furthermore, because the refresh operation is internal to each SLM cell 50, refresh operation may occur more often than conventional arrangements, an advantage that permits the size of each capacitor 52 to be even smaller. Specification, p. 4.

For purposes of updating the memory 66 with a new value that indicates the pixel intensity of the next frame, a word, or row, line 56 that is associated with the row of the SLM cell 50 is asserted (driven high, for example) to cause the memory 66 to load the new data from the corresponding bit lines 57. At this time, sense amplifiers 58 respond to the new bit values to store the new values into bit latches 60 that store the bit values for conversion by the DAC 62. In this manner, the DAC 62 converts the digital value that is indicated by the bits into an analog voltage that appears on an analog line 64 that is coupled to a plate of the pixel cell 54. The other plate of the pixel cell 54 may be coupled to ground. Specification, pp. 4-5.

The refresh operation also uses the sense amplifiers 58, the bit latches 60 and the DAC 62. In this manner, a refresh signal line 59 may be asserted (driven high, for example) to indicate the refresh operation. When the word line 56 is also asserted, the sense amplifiers 58 generate signals to store bits (in the bit latches 60) that indicate the value that is stored in the memory 66. The DAC 62 then converts the digital value that is indicated by the bits into the analog voltage that appears on the line 64. Specification, p. 5.

As an example, in some embodiments, the SLM cell 50 may be refreshed at a rate of approximately 1 KHz to minimize the appearance of an artifact, or error, when the SLM cell 50 is updated with the intensity value for the next frame. In some embodiments, the frame update occurs between the read cycle of the refresh operation. Therefore, for purposes of writing an indication of a new pixel intensity in the memory 66 for the next frame, the write operation may be synchronized with the refresh clock signal and then written into the memory 66 between two refresh cycles. Because the rate at which the memory 66 is updated is much lower than the refresh rate, there is always enough cycle to write new data into the memory 66. Specification, p. 5.

Referring to Fig. 3, the SLM cell 50 may be used in an SLM 200 and may be one of several SLM cells 50 that are arranged in rows and columns. In some embodiments, the SLM 200 may include a row decoder 208 that includes control lines 214 to select a particular row of SLM cells 50 for raster scan updates or a refresh operation, and the SLM 200 may include a column decoder 204 that includes control and data lines 212 to update the memories 66 of a group of the SLM cells 50 of a particular row. In this manner, in some embodiments, to perform a raster scan, the row decoder 208 may select the SLM cells 50 one row at a time. For each selected row, the column decoder 204 selects a group of the SLM cells 50, updates the memories of the selected group of SLM cells 50 and continues this process until the memories of all of the SLM cells 50 of the selected row have been updated. Other arrangements are possible. Specification, p. 5.

In some embodiments of the invention, the SLM cells 50 may be arranged in a rectangular array 201 of units 207. In this manner, each unit 207 may include a block of

thirty-two columns by sixteen rows of SLM cells 50. The SLM cells 50 of a particular unit 207 share sense amplifiers 58, bit latches 60 and DACs 62 that function as described above. A multiplexer 51 (of each unit 207) selectively couples the SLM cells 50 of a particular row of the block to the sense amplifiers 58 to perform a particular refresh operation, for example. A demultiplexer 53 (of each unit 207) selectively couples the output terminals 64 to the selected row of SLM cells 50 to complete the particular refresh operation, for example. To accomplish these features, each SLM cell 50 is coupled to the multiplexer 51 of its unit 207 via conductive lines 67. Specification, p. 6.

Referring to Fig. 4, in some embodiments, the DACs 62 for a particular unit 207 may be part of a circuit 298. The circuit 298 may be associated with a block of thirty-two columns by sixteen rows of SLM cells 50. In this manner, in each refresh operation, the circuit 298 operates on the associated SLM cells 50 that are in a particular row. Thus, for the example above, in some embodiments of the invention, the circuit 298 performs the digital-to-analog conversions for thirty-two SLM cells 50 at time. Specification, p. 6.

As an example, in some embodiments of the invention, the circuit 298 may include a resistor divider 300 that is formed from resistors 301 that are serially coupled between a reference voltage (called V_{REF}) and ground. The terminals of the resistors 301 provide reference voltages that the second stages 304 of the various DACs 62 use to furnish their analog signals based on the values that are stored in the respective memories 66. As an example, each second stage 304 may include a multiplexer 307 that has input terminals 308 that are coupled to receive indications of the bits from the SLM cells 50 of the unit 207. In this manner, each multiplexer 307 is associated with a different column

and selects the bits from the memory 60 of an SLM cell 50 of the selected row. The multiplexer 307 directs indications of these bits into a decoder 310. The decoder 310, in turn, operates switches 312 that receive the voltage across one of the resistors 301. The switches 312 furnish an analog voltage that is proportional to the value that is indicated by the bits, and an analog interface 314 scales this voltage before providing the voltage to a demultiplexer 316 that furnishes the scaled analog voltage to the appropriate capacitor 52. Thus, due to the above-described arrangement, each DAC 62 includes the resistor divider 300 (that forms the first stage) and the second stage 304. Specification, pp. 6-7.

VI. ISSUES

A. Can claims 45-49 and 53 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 45?

B. Can claims 50-52 and 54 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 50?

VII. GROUPING OF THE CLAIMS

Claims 45-49 and 53 can be grouped together; and claims 50-52 and 54 can be grouped together. With this grouping, all claims of a particular group stand or fall together. Furthermore, regardless of the grouping set forth by the Examiner's rejections, the claims of each group set forth in the section stand alone with respect to the other groups. In other words, any claim of a particular group set forth in this section, does not stand or fall together with any claim of any other group set forth in this section.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 45-49 and 53 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 45?

The method of independent claim 45 includes providing a light modulator that includes an array of pixel cells and memory buffers. Each memory buffer is associated with a different group of two or more of the pixel cells; and each memory buffer is located closer to the associated group of pixel cells than another one of the group of pixel cells. The method includes during a refresh operation, converting the digital indication stored in the memory buffers into analog voltages to update charge intensities on the pixel cells.

The Examiner rejects independent claim 45 under 35 U.S.C. § 103(a) over U.S. Patent No. 6,333,737 (herein called "Nakajima") in view of U.S. Patent No. 6,297,787 (herein called "Nishida"). Nakajima generally discloses a liquid crystal display that is formed on an integrated circuit. This device includes memory and control circuitry (see Figure 1, for example) for each pixel of the device. Nakajima states that the disclosed structure operates at a very high speed and states the advantages of each pixel instantaneously operationally processing a particular digital signal so that information related to this digital signal is displayed on the pixel. *See, for example,* Nakajima, 6:13-24 and 40-52. There is no teaching or suggestion in Nakajima regarding modifying the disclosed structure so that its memories 22 are associated with different groups of pixel

cells and locating each memory 22 closer to the associated group of pixel cells than to another one of the group of pixel cells.

Nishida discloses an electric bulletin board that includes electric light bulbs for its display elements. In particular, Nishida is directed to reducing the wiring that is associated with electric bulletin boards. Nishida describes display units that are individually mass produced and assembled to form the electric bulletin board. See, *for example,* Nishida, 7:42-58. In lines 43-60 in column 13 of Nishida, Nishida states that a particular display unit may include several pixels that share the same controller and memory.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 45 for at least the reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation for the modification of Nakajima's integrated display device in view of Nishida. More specifically, the § 103 rejection of claim 45 relies on the modification of Nakajima's integrated display device so that the display device includes memories that are associated with multiple pixel cells and are located closer to the associated group of pixel cells than to the other groups of pixel cells. However, the Examiner fails to show where the prior art contains the alleged suggestion or motivation, a requirement for a *prima facie* case of obviousness, for this proposed modification of Nakajima. M.P.E.P. § 2143.

In an attempt to show this alleged suggestion or motivation, the Examiner states in the Final Office Action that the alleged suggestion or motivation for the combination stems from the need, "to reduce the cost and complexity needed to provide a separate

memory at each single pixel while still providing the advantages of the invention in Nakajima." Final Office Action, 6-7. However, the Examiner provides no support as to why modifying Nakajima's integrated display device in this manner would reduce the cost and complexity of Nakajima's device. The problems and solutions that are presented in Nishida relate to reducing the possible cost associated with the mass production of individual display units do not apply to the integrated display structure that is disclosed in Nakajima. In fact, modification of Nakajima's integrated display device, as contended by the Examiner, would arguably result in more cost and complexity in Nakajima's device, as each memory 22 would serve more than one pixel. Thus, contrary to the Examiner's position, arguably cost and complexity would be added to Nakajima's display device by the proposed modification.

The Examiner, in the Final Office Action also cites general language from Nakajima to allegedly show this suggestion or motivation for the modification of Nakajima. This language merely states that various modifications may be made. However, none of this language provides a teaching or suggestion to modify Nakajima's display device so that the memory 22 is used by more than one pixel cell.

Nishida discloses each display unit may have a single memory and multiple pixels. However, this disclosure provides no suggestion or motivation for one skilled in the art, *without knowledge of the claimed invention*, to modify Nakajima's integrated display device so that this device includes multiple memories that are associated with multiple groups of pixel cells.

Additionally, the Examiner has not shown where the combination of references teaches or suggests a memory buffer that is located closer to an associated group of pixel cells than another group of pixel cells. All claim limitations must be considered when judging the patentability of a claim over the prior art. M.P.E.P. § 2143.01. Thus, the Examiner has ignored the limitations of claim 45 reciting that each memory buffer is located closer to the associated group of pixel cells than to another group of pixel cells. Applicants submit that such a teaching is neither explicitly, implicitly or inherently taught by Nishida.

More specifically, Nishida is not specific as to the location of the memory in a particular display unit. Therefore, even assuming, for purposes of argument, that each display unit contains multiple pixel cells for a single memory, the memory of one particular display unit may be physically closer to the group of pixel cells of the adjacent display unit, for example, than to the pixel cells in its own unit.

"Obviousness cannot be predicated on what is unknown." Thus, the Examiner must provide citations to a prior art reference that establishes the alleged suggestion or motivation to combine and/or modify references to derive the claimed invention; and the Examiner must show where the prior art teaches or suggests all claim limitations. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. In the Final Office Action, the Examiner cites *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988). However, contrary to the Examiner's position, *In re Fine* further supports the Applicant's position that a *prima facie* case of obviousness has not been established for independent claim 45.

More specifically, in *In re Fine*, the Federal Circuit held that the Examiner had failed to establish a *prima facie* case of obviousness because of the Examiner's bald assertion that a substitution "would have been within the skill of the art," without offering any support for or explanation of this conclusion. *In re Fine*, 5 USPQ2d at 1599. The Federal Circuit agreed with the appellant that a *prima facie* case of obviousness had not been established and stated, "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *Id.*, 1600. *See also, W.L. Gore & Associates, Inc v. Garlock, Inc.,* 220 USPQ 303, 312-13 (Fed. Cir. 1983) (stating, " to imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against his teacher"); *Al-Site Corp. v. VSI Int'l, Inc.,* 50 USPQ2d 1161, 1171 (Fed. Cir. 1999) (stating, " rarely, however, will the skill in the art component operate to supply missing knowledge or prior art to reach an obviousness judgment").

Thus, a *prima facie* case of obviousness has not been established for independent claim 45 for at least the reasons that are set forth above. Claims 46-49 and 53 are patentable for at least the reason that these claims depend from an allowable claim.

Therefore, the § 103 rejections of claims 45-49 and 53 are in error and should be reversed.

B. Can claims 50-52 and 54 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 50?

The light modulator of independent claim 50 includes an array of pixel cells, memory buffers, and digital-to-analog converters. The memory buffers are spatially distributed among the pixel cells with each memory buffer being associated with a different group of two or more of the pixel cells and storing digital indications of associated predetermined voltages. The digital-to-analog converters convert the digital indications into analog voltages to update charges on the pixel cells during a refresh operation.

The Examiner rejects independent claim 50 under 35 U.S.C. § 103(a) over Nakajima in view of Nishida. More specifically, the Examiner's rejections relies on the modification of Nakajima's integrated circuit device so that instead of having a single memory 22 for each pixel cell, this integrated display device includes a memory for each group of pixel cells.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 50 for at least the reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation for the modification of Nakajima in view of Nishida. A *prima facie* case of obviousness requires more than just a piecewise combination of elements from various references. Rather, the Examiner must show the existence of alleged suggestion or motivation in the prior art in order to establish a *prima facie* case of obviousness. M.P.E.P. § 2143; *see, Ex parte Gambogi*, 62 USPQ2d 1209,

1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

More specifically, the Examiner fails to establish where the prior art contains the alleged suggestion or motivation to modify Nakajima so that its display device includes multiple memory buffers that are each associated with groups of two or more pixel cells. Furthermore, the Examiner fails to show where the prior art contains the alleged suggestion or motivation to modify Nakajima so that Nakajima's integrated display device includes memory buffers that are spatially distributed among the pixel cells.

Thus, for at least any one of these reasons, a *prima facie* case of obviousness has not been established for independent claim 50. Claims 51-52 and 54 are patentable for at least the reason that these claims depend from an allowable claim.

Therefore, the § 103(a) rejections of claims 50-52 and 54 are in error and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: April 30, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

45. A method comprising:

providing a light modulator comprising an array of pixel cells and memory buffers, each memory buffer being associated with a different group of two or more of the pixel cells and each memory buffer being located closer to the associated group of pixel cells than another one of the group of pixel cells; and

during a refresh operation, converting the digital indications stored in the memory buffers into analog voltages to update charge intensities on the pixel cells.

46. The method of claim 45, wherein the memory buffers are localized to the different groups.

47. The method of claim 45, wherein the memory buffers comprise ~~a~~ static random access memories.

48. The method of claim 45, further comprising:

during the refresh operation, reading the digital indications from the memory buffers.

49. The method of claim 45, further comprising:

during the refresh operation, latching the digital indications.

50. A light modulator comprising:

an array of pixel cells;

memory buffers being spatially distributed among the pixel cells, each memory buffer being associated with a different group of two or more of the pixel cells and storing a digital indications of associated predetermined voltages; and

digital-to-analog converters to convert the digital indications into analog voltages to update charges on the pixel cells during a refresh operation.

51. The light modulator of claim 50, wherein the refresh operation occurs at a different rate than a frame update operation to the pixel cells.

52. The light modulator of claim 50, wherein at least one of the memory buffers comprise static random access memory.

53. The method of claim 45, wherein each of the pixel cells is controlled independently with respect to the other pixel cells.

54. The light modulator of claim 50, wherein each of the pixel cells is controlled independently with respect to the other pixel cells.